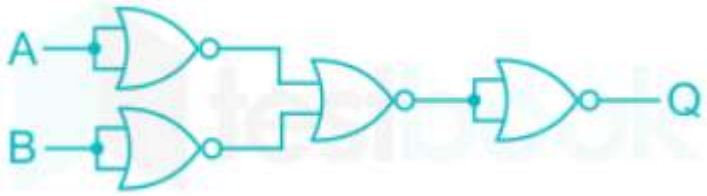
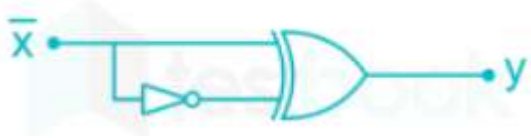
EC1002 – APPLIED DIGITAL LOGIC DESIG

Set 1

Q.NO.		ANS
1	If we add an inverter at the output of AND gate, what function is produced? a)XOR b)NAND c)OR d)NOR	b
2	OR gate and------- will form the NOR gate? a)OR b)NAND c)AND d)NOT	d
3	What are the canonical forms of Boolean expressions? a)OR and XOR b) NOR and XNOR c)MAX and MIN d)SOP and POS	d
4	The Boolean expression AB+AC'+BC simplifies to a)BC+AC' b)AB+AC'+B c)AB+AC' d)AB+BC	a
5	The output of the logic circuit given below represents _____ gate.  a)OR b)NOR c)AND d)NAND	d
6	The output Y of the logic circuit given below is:  a)1 b)0 c)X d)X'	a
7	The minimum number of NAND gates required to realise AB+AB'C+AB'C' is	d

	a)3 b)2 c)1 d)0	
8	—---------- are universal logic gates. a) NAND and NOR b) NOR AND EX-OR c) AND and NOT d) OR and EX-OR	**A**
9	One operation that is not given by magnitude comparator is a) Equal b) Less than c) Greater than d) Sum	
10	Adding 1001 and 0010 gives the output of a) 1011 b) 1111 c) 1010 d) 0000	
11	Major difference between half-adders and full-adders is a) Full-adders are made up of two half-adders b) Full-adders can handle double digit numbers c) Full-adders have carry input capability d) None	
12	Binary subtraction of 0-1 yields a) Difference = 0, borrow = 0 b) Difference = 1, borrow = 0 c) Difference = 1, borrow = 1 c) Difference = 0, borrow = 1	
13	How many basic binary subtraction operations are possible? a) 1 b) 4 c) 3 d) 2	
14	What are the two types of basic adder circuits? a) Sum and carry b) Half-adder and full-adder c) Asynchronous and synchronous d) One and two’s-complement	
15	Which of the following is correct for full adders? a) Full adders have the capability of directly adding decimal numbers b) Full adders are used to make half adders	

	c) Full adders are limited to two inputs since there are only two binary digits d) In a parallel full adder, the first stage may be a half adder	
16	If A and B are the inputs of a half adder, the sum is given by __ a) A AND B b) A OR B c) A XOR B d) A EX-NOR B	
17	The correct combination of characteristic equation Q_{n+1} of S-R flip flop is a. $\overline{\mathrm{S}} + \overline{\mathrm{R}}Q_n$ b. $\overline{\mathrm{S}} + \mathrm{R}\overline{Q_n}$ c. $\mathrm{S} + \overline{\mathrm{R}}Q_n$ d. $\mathrm{S} + \mathrm{R}Q_n$	c
18	The correct combination of characteristic equation Q_{n+1} of J-K flip flop is- a. $\mathrm{J}\overline{\mathrm{Q_n}} + \overline{\mathrm{K}}\mathrm{Q_n}$ b. $\mathrm{J}\mathrm{Q_n} + \mathrm{K}\mathrm{Q_n}$ c. $\overline{\mathrm{J}}\mathrm{Q_n} + \mathrm{K}\overline{\mathrm{Q_n}}$ d. $\mathrm{J}\overline{\mathrm{Q_n}} + \overline{\mathrm{K}}\mathrm{Q_n}$	a
19	The correct combination of characteristic equation Q_{n+1} of T flip flop is a. $\mathrm{T}\mathrm{Q_n} + \mathrm{T}\overline{\mathrm{Q_n}}$ b. $\overline{\mathrm{T}}\mathrm{Q_n} + \mathrm{T}\overline{\mathrm{Q_n}}$ c. $\overline{\mathrm{T}}\mathrm{Q_n} + \overline{\mathrm{T}\mathrm{Q_n}}$ d. $\mathrm{T}\overline{\mathrm{Q_n}} + \mathrm{T}\overline{\mathrm{Q_n}}$	b

20	The correct combination of characteristic equation Q_{n+1} of D flip flop is- a. D b. DQ_n c. $\overline{D}$ $D\overline{Q_n}$	a

Set 2

Q.NO.		**ANS**
1	Which of the following logic gates provides output as 0 when both inputs are the same (either 0 or 1)? a) XNOR b)XOR c)NOR d)NAND	**b**
2	An XNOR gate produces an output only when the two inputs are: a)High b)Different c)Low d)Same	**d**
3	The octal equivalent of 1100101.001010 is a)624.12 b)145.12 c)154.12 d)145.21	**b**
4	Convert the binary equivalent 10101 to its decimal equivalent a)21 b)12 c)22 d)31	**a**
5	Which of the following is not a binary number a)111 b)101 c)11E d)000	**c**

6	What could be the maximum value of a single digit in an octal number system? a) 8 b)7 c)6 d)5	**b**
7	The maximum number of bits sufficient to represent an octal number in binary is a) 4 b)3 c)7 d)8	**b**
8	Convert $(22)_8$ into its corresponding decimal number. a) 28 b)18 c)81 d)82	**b**
9	If A and B are the inputs of a half adder, the carry is given by a) A AND B b) A OR B c) A XOR B d) A EX-NOR B	**a**
10	Half-adders have a major limitation in that they cannot _____ a) Accept a carry bit from a present stage b) Accept a carry bit from a next stage c) Accept a carry bit from a previous stage d) Accept a carry bit from the following stages	**c**
11	If A, B and C are the inputs of a full adder then the carry is given by _____ a) A AND B OR (A OR B) AND C b) A OR B OR (A AND B) C c) (A AND B) OR (A AND B) C d) A XOR B XOR (A XOR B) AND C	**a**
12	How many AND, OR and EXOR gates are required for the configuration of full adder? a) 2, 2, 2 b) 2, 1, 2 c) 3, 1, 2 d) 4, 0, 1	**a**
13	Let the input of a subtractor is A and B then what the output will be if A = B? a) 0 b) 1 c) A d) B	**a**
14	Let A and B is the input of a subtractor then the output will be	**a**

	a) A XOR B b) A AND B c) A OR B d) A EXNOR B	
15	Full subtractor is used to perform subtraction of _____ a) 2 bits b) 3 bits c) 4 bits d) 8 bits	**b**
16	The full subtractor can be implemented using _____ a) Two XOR and an OR gates b) Two half subtractors and an OR gate c) Two multiplexers and an AND gate d) Two comparators and an AND gate	**b**
17	A sequential circuit design is used to _____ a. Count up b. Count down c. Decode an end count d. Count in a random order	d
18	The minimum number of flip-flops that can be used to construct a modulus-5 counter is _____ a. 3 b. 8 c. 5 d. 10	a
19	Normally, the synchronous counter is designed using ____ a. S-R flip-flops b. J-K flip-flops c. D flip-flops d. T flip-flops	b

20	What is a state diagram? a. It provides the graphical representation of states b. It provides exactly the same information as the state table c. It is same as the truth table d. It is similar to the characteristic equation	b

Set 3

Q.NO.		**ANS**
1	Which of the following is the correct representation of a binary number? a) $(124)_2$ b)1110 c) $(110)^2$ d)$(000)_2$	**d**
2	Which out of the following binary number is equivalent to decimal number 24 a)1101111 b)11000 c)111111 d)110011	**b**
3	The number of digits required to represent a decimal number 31 in equivalent binary form a)2 b)4 c)5 d)6	**c**
4	The octal equivalent of 110001011100 is a) 6134 b) 5264 c) 6258 d) 5023	**a**
5	Convert $(64)_{16}$ into its corresponding binary number	**b**

	a) 1101100 b)1100100 c)111000 d)01011110	
6	Simplify Y = AB’ + (A’ + B)C. a) AB’ + C b) AB + AC c) A’B + AC’ d) AB + A	**a**
7	The Boolean expression for a 3-input AND gate is _____. A. X = AB B. X = ABC C. X = A + B + C D. X = AB + C	**b**
8	Which of the following binary number is equivalent to decimal number 24 a) 11000 b) 1101111 c) 101011 d) 11100	**a**
9	The output of a full subtractor is same as _____ a) Half adder b) Full adder c) Half subtractor d) Decoder	**b**
10	Fast-look-ahead carry circuits found in most 4-bit full-adder circuits which _____ a. Determine sign and magnitude b. Reduce propagation delay c. Add a 1 to complemented inputs d. Increase ripple delay	**b**

11	One way to make a four-bit adder to perform subtraction is by a. Inverting the output b. Inverting the carry-in c. Inverting the B inputs d. Grounding the B inputs	**c**
12	What distinguishes the look-ahead-carry adder? a. It is slower than the ripple-carry adder b. It is easier to implement logically than a full adder c. It is faster than a ripple-carry adder d. It requires advance knowledge of the final answer	**c**
13	Carry lookahead logic uses the concepts of _____ a. Inverting the inputs b. Complementing the outputs c. Generating and propagating carries d. Ripple factor	**d**
14	A circuit that converts n inputs to 2n outputs is called a. Encoder b. Decoder c. Comparator d. Adder	**b**
15	Encoders can be made by three a. AND gates b. OR gates c. XOR gates d. XNOR gates	**b**
16	How many 3:8 line decoders with enable input line are required to 6:64 line decoder without using any other logic gates? a. 7	**b**

	b. 9 c. 8 d. 10	
17	The expression for MOD number for a ripple counter with N flip-flops is a. N b. 2^N c. 2^{N-1} d. 2^N-1	b
18	Propagation delay of flip flops used for counter design largely affects the speed of operation of- a. Asynchronous (ripple) counter b. Synchronous up counter c. Synchronous down counter Synchronous up down counter	a
19	In _____, the flip-flop output transition serves as a source for triggering other flip-flops. a. Shift register b. Ripple counter c. Serial adder d. Parallel adder	b
20	A ripple counter with n flip-flops can function as a – a. n:1 counter b. n/2:1 counter c. 2n:1 counter	d

	d. 2^n:1 counter	

Set 4

Q.NO.		ANS
1	The base of hexadecimal number system is a) 2 b) 8 c) 10 d) 16	**d**
2	How many AND gates are required to realise Y = CD + EF + G? a) 4 b)5 c)3 d) 2	**d**
3	What can eliminate two variables and their complements? a)pair b)quad c)octet d)overlapping group	**b**
4	The simplified SOP (Sum of product) form of the boolean expression (P+Q'+R').(P+Q'+R).(P+Q+R') is a) (P'.Q+R') b) (P+Q'.R') c) (P'.Q+R) d) (P.Q+R)	**b**
5	The output of a logic gates is 1 when all its inputs are at logic 0 the gate is either a)NAND or EX-OR b)OR or EX-NOR c)AND or EX-or d)NOR or EX-NOR	**d**

6	How many NAND gates and NOT gates are required for the construction of EXOR. a) 3,4 b) 4,5 c) 5,4 4,3	**b**
7	Which of the following expressions does not represent exclusive NOR of x and y? a)xy+x'y' b)x XOR y' c)x' XOR y d)x' XOR y'	**d**
8	A3 variable karnaugh map has _____ a. Eight cells b. Three cells c. Sixteen cells d. Four cells	**a**
9	Which of the following can be represented for decoder? a. Sequential circuit b. Combinational circuit c. Logical circuit d. None of the mentioned	**b**
10	BCD to seven segment conversion is a _____ a. Decoding process b. Encoding process c. Comparing process d. None of the mentioned	**a**
11	Decoder is constructed from _____ a. Inverters	**c**

	b. AND gates c. Inverters and AND gates d. None of the mentioned	
12	Which of the following represents a number of output lines for a decoder with 4 input lines? a. 15 b. 16 c. 17 d. 18	**b**
13	Decoders and Encoders are doing reverse operation. a. True b. False	**a**
14	If we record any music in any recorder, such types of process is called _____ a. Multiplexing b. Encoding c. Decoding d. Demultiplexing	**b**
15	Can an encoder be a transducer? a. Yes b. No c. May or may not be d. Both are not even related	**a**
16	How many combinations are possible for 8-bit input encoder? a. 8 b. 2^8 c. c4 d. 2^4	**b**

17	Which shift register counter required the most decoding circuitry? a. Johnson counter b. Ring counter c. Ripple counter d. MOD counter	c
18	Maximum count value of a n bit counter is- a. 2^n-1 b. 2^n c. 2^{2n} d. 2^n+1	a
19	In which one of the following counters, the flip flops are not clocked simultaneously? a. Synchronous counter b. Asynchronous counter/ripple counter c. Both a and b d. None of the above	b
20	In which one of the following one the output will always follow a sequence either in downward or upward direction? a. Counters b. Registers c. Both a and b d. None of the above	a

Set 5

Q.NO.		ANS
1	An OR gate has 4 inputs.One input is high and the other three are low the output is a) Low b) High c) alternately high and low d) may be high or low depending on relative magnitude of inputs	b
2	Express the Boolean function F = A + B'C as standard sum of minterms. a)Sigma(1, 4, 5, 6, 7) b)Sigma(2, 3, 5, 8, 9) c)Sigma(1, 2, 4, 6, 8) d)Sigma(1, 3, 4, 5, 7)	a
3	Tabular column is also known as_____method a)Karnaugh map b)Quine Mc Cluskey c)Prime Implicant d)None of the above.	b
4	Complement of the expression A'B + CD' is _____ a) (A' + B)(C' + D) b) (A + B')(C' + D) c) (A' + B)(C' + D) d) (A + B')(C + D')	b
5	The minterm expression of f(P,Q,R)=PQ+QR'+PR' is A.)m2+m4+m6+m7 B.)m0+m1+m3+m5 C.)m0+m1+m6+m7	a

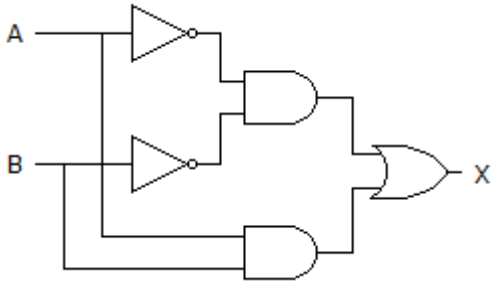
	D.)m2+m3+m4+m5	
6	The observation that a bubbled input OR gate is interchangeable with a bubbled output AND gate is referred to as _____. a) A Karnaugh map b) Demorgan's second theorem c) Commutative law of addition d) Associative law of multiplication	**b**
7	What is the equivalent of (+)ve AND using assertion level logic? a)(-)ve OR b)(+)ve OR c)(-)ve NAND d)(+)ve NAND	**a**
8	Which of the following is a SOP equation? a)(A+B)(A+C) b)AB+AC c) Both a and b d) NOT A	**a**
9	Can an encoder be called a multiplexer? a. No b. Yes c. Sometimes d. Never	**b**
10	A digital multiplexer is a combinational circuit that selects a. One digital information from several sources and transmits the selected one b. Many digital information and convert them into one c. Many decimal inputs and transmits the selected information d. Many decimal outputs and accepts the selected information	**a**

11	4 to 1 MUX would have _____ a. 2 inputs b. 3 inputs c. 4 inputs d. 5 inputs	**c**
12	The two input MUX would have _____ a. 1 select line b. 2 select lines c. 4 select lines d. 3 select lines	**a**
13	Which of the following circuit can be used as parallel to serial converter? a. Multiplexer b. Demultiplexer c. Decoder d. Digital counter	**a**
14	How many select lines would be required for an 8-line-to-1-line multiplexer? a. 2 b. 4 c. 8 d. 3	**a**
15	In a multiplexer the output depends on its _____ a. Data inputs b. Select inputs c. Select outputs d. Enable pin	**b**
16	In 1-to-4 multiplexer, if C1 = 0 & C2 = 1, then the output will be _____	**b**

	a. Y0 b. Y1 c. Y2 d. Y3	
17	The synchronous counter is also called a parallel counter. a. True b. False	a
18	In asynchronous counter, the maximum frequency of operation is low compared to parallel counter. a. True b. False	a
19	Other name for Asynchronous counters is _____counters. a. Ripple b. Up counter c. Down counter d. Modulous	a
20	How many types of the counter are there? a. 2 b. 3 c. 4 d. 5	a

Set 6

Q.NO.		ANS
1	The boolean function A+BC is a reduced form of a)AB+BC b)(A+B)(A+C) c)A'B+AB'C d)(A+C)B	**b**
2	How many AND gates are required to realize Y = CD + EF + G? a) 4 b) 5 c) 3 d) 2	**d**
3	If a 3-input NOR gate has eight input possibilities, how many of those possibilities will result in a HIGH output? a)1 b) 2 c) 7 d) 8	**a**
4	The inverter is .. a) NOT GATE b) NOR GATE c)AND GATE d) OR GATE	**a**
5	An exclusive NOR gate is logically equal to a.inverter followed by an XOR gate b.NOT gate followed by an exclusive XOR gate c.Exclusive OR gate followed by an inverter d.Complement of NOR gate	**c**
6	If a three variable switching function is expressed as the product of maxterms by f(A,B,C) = π(0,3,5,6) then it can also be expressed as sum of min terms by a) π(1,2,4,7) b) Σ(0,3,5,6) c) Σ(1,2,4,7) d) Σ(1,2,3,7)	**c**

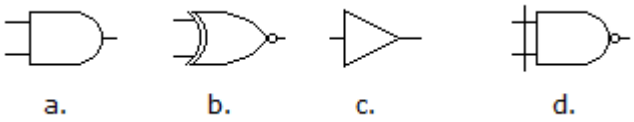
7	Canonical is a unique way of representing_____ a)SOP b)Minterm c)Boolean Expressions d)POS	**c**
8	Which of the following logic expressions represents the logic diagram shown?  a) X=AB'+A'B b) X=(AB)'+AB c) X=(AB)'+A'B' d) X=A'B'+AB	**d**
9	How many AND gates are required for a 1-to-8 multiplexer? a. 2 b. 6 c. 8 d. 5	**c**
10	Latch is a device with _____ stable states a. one b. two c. three d. infinite	**b**
11	The truth table for an S-R flip-flop has how many VALID entries?	**c**

	a) 1 b) 2 c) 3 d) 4	
12	A basic S-R flip-flop can be constructed by cross-coupling of which basic logic gates? a) AND or OR gates b) XOR or XNOR gates c) NOR or NAND gates d) AND or NOR gates	**c**
13	The basic latch consists of _____ a) Two inverters b) Two comparators c) Two amplifiers d) Two adders	**a**
14	When both inputs of SR latches are low, the latch _____ a) Q output goes high b) Q' output goes high c) It remains in its previously set or reset state d) it goes to its next set or reset state	**c**
15	When the J and K inputs are low, the state of the outputs Q and Q' are a. unchanged on clocking b. changed on clocking c. changed on output d. changed on input	**a**
16	Which among the following is not a mode of Flip Flop representation? a. Characteristic Equations	**d**

	b. Excitation Tables c. Finite State Machines (FSM) d. Variable Entered Mapping (VEM)	
17	A shift register is a digital circuit that _____ . a. Stores data b. Shifts the data from left to right c. Shifts the data from right to left d. All the mentioned	d
18	What is a shift register? a. An adder circuit b. A memory circuit c. A combinational circuit d. A decoder circuit	b
19	Shift register is a Digital type of register. a. True b. False	a
20	A shift register is made up of how many flip-flops? a. One b. Two c. Three or more d. None of the above	c

Set 7

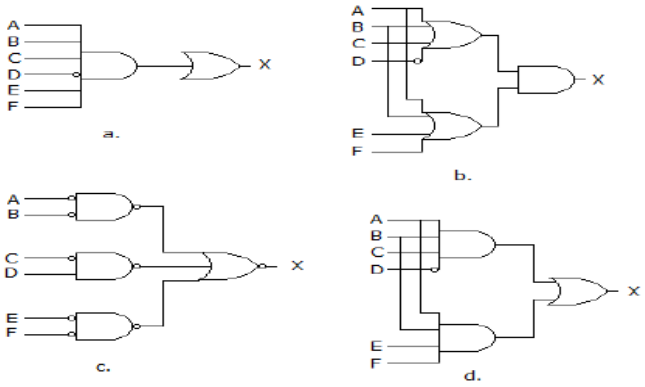
Q.NO.		ANS
1	DeMorgan's theorem states that_____ a)(AB)'=A'+B' b)(A+B)'=A'*B c)A'+B'=A'B' d)(AB)'=A'+B	a
2	Which of the following is an incorrect SOP expression? A. (a+b)(a+c) B. a+b C. b+a.c D. b'c'+bc'	a
3	1's complement of binary number is obtained by changing a) Each 1 to 0 b) Each 0 to 1 c) Each 1 to 0 and 0 to 1 None of the above	c
4	The octal equivalent of the decimal number (417)10 is _____ a) $(641)_8$ b) $(619)_8$ c) $(640)_8$ d) $(598)_8$	a
5	The decimal equivalent of the binary number (1011.011)2 is _____ a) $(11.375)_{10}$ b) $(10.123)_{10}$ c) $(11.175)_{10}$ d) $(9.23)_{10}$	a

6	The largest two digit hexadecimal number is _____ a) (FE)16 b) (FD)16 c) (FF)16 d) (EF)16	**c**
7	Representation of hexadecimal number (6DE)H in decimal: a) $6 * 16^2 + 13 * 16^1 + 14 * 160$ b) $6 * 16^2 + 12 * 16^1 + 13 * 160$ c) $6 * 16^2 + 11 * 16^1 + 14 * 160$ d) $6 * 16^2 + 14 * 16^1 + 15 * 160$	**a**
8	Which of the figures shown below represents the exclusive-NOR gate?  a. b. c. d.	B
9	The full form of SR is a) System rated b) Set reset c) Set ready d) None of the Mentioned	**b**
10	In a J-K flip-flop, if J=K the resulting flip-flop is referred to as a) D flip-flop b) S-R flip-flop c) T flip-flop d) S-K flip-flop	**c**
11	The only difference between a combinational circuit and a flip-flop is that _____	**c**

	a) The flip-flop requires previous state b) The flip-flop requires next state c) The flip-flop requires a clock pulse d) The flip-flop depends on the past as well as present states	
12	The flip-flop is only activated by _____ a) Positive edge trigger b) Negative edge trigger c) Either positive or Negative edge trigger d) Sinusoidal trigger	**c**
13	The S-R latch composed of NAND gates is called an active low circuit because a) It is only activated by a positive level trigger b) It is only activated by a negative level trigger c) It is only activated by either a positive or negative level trigger d) It is only activated by sinusoidal trigger	**b**
14	Both the J-K and T flip-flop are derived from the basic _____ a) S-R flip-flop b) S-R latch c) D latch d) D flip-flop	**b**
15	The flip-flops which do not have any invalid states are _____ a) S-R, J-K, D b) S-R, J-K, T c) J-K, D, S-R d) J-K, D, T	**d**
16	What does the triangle symbol on the clock input of a J-K flip-flop mean?	**b**

	a) Level enabled b) Edge triggered c) Both Level enabled; Edge triggered d) Level triggered	
17	A shift register can have _____ data input and _____ data output lines. a. Only one, only one b. Two, two c. One, two d. Three, two	c
18	The full form of SIPO is _____ a. Serial-in Parallel-out b. Parallel-in Serial-out c. Serial-in Serial-out d. Serial-In Peripheral-Out	a
19	The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains _____ a. 01110 b. 00001 c. 00101 d. 00110	c
20	Which type of shift register is used to implement a digital up-down counter? a. SISO b. SIPO c. PISO d. PIPO	a

Set 8

Q.NO.		ANS
1	Which of the circuits in figure (a to d) is the sum-of-products implementation of figure (e)?  	D
2	Single looping in groups of three is a common K-map simplification technique. A True B False	B
3	In true sum-of-products expressions, the inversion signs cannot cover more than single variables in a term. True B) False	A
4	A combinatorial logic circuit has memory characteristics that "remember" the inputs after they have been removed A)True B) False	B

5	A Karnaugh map will _____. A eliminate the need for tedious Boolean simplifications B allow any circuit to be implemented with just AND and OR gates C produce the simplest sum-of-products expression D give an overall picture of how the signals flow through the logic circuit	A
6	One reason for using the sum-of-products form is that it can be implemented using all _____ gates without much difficulty. A NOR B NAND C AND D DOOR	B
7	The output of a gate has an internal short; a current tracer will _____. A. identify the defective gate B. show whether the gate is shorted to V_{cc} or ground C. probably not be able to locate the problem D. be able to identify the defective load node	A

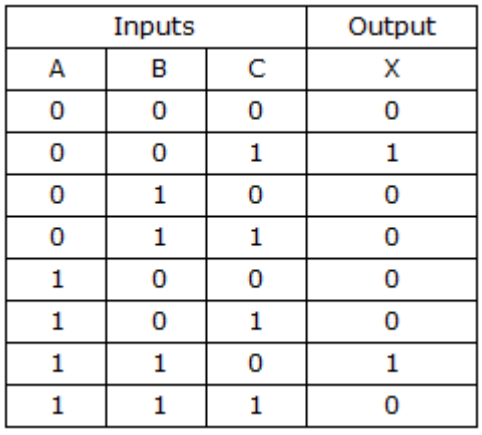
8	A gate that could be used to compare two logic levels and provide a HIGH output if they are equal is a(n) _____. A XOR gate B. XNOR gate C. NAND gate D NOR gate	B
9	On a positive edge-triggered S-R flip-flop, the outputs reflect the input condition when a) The clock pulse is LOW b) The clock pulse is HIGH c) The clock pulse transitions from LOW to HIGH d) The clock pulse transitions from HIGH to LOW	**c**
10	D flip-flop is a circuit having _____ a) 2 NAND gates b) 3 NAND gates c) 4 NAND gates d) 5 NAND gates	**c**
11	In a positive edge triggered JK flip flop, a low J and low K produces? a) High state b) Low state c) Toggle state d) No Change State	**d**
12	S-R type flip-flop can be converted into D type flip-flop if S is connected to R through _____	**c**

	a) OR Gate b) AND Gate c) Inverter d) Full Adder	
13	The term synchronous means _____ a) The output changes state only when any of the input is triggered b) The output changes state only when the clock input is triggered c) The output changes state only when the input is reversed d) The output changes state only when the input follows it	**b**
14	The S-R, J-K and D inputs are called _____ a) Asynchronous inputs b) Synchronous inputs c) Bidirectional inputs d) Unidirectional inputs	**b**
15	For realisation of JK flip-flop from SR flip-flop, the input J and K will be given as _____ a) External inputs to S and R b) Internal inputs to S and R c) External inputs to combinational circuit d) Internal inputs to combinational circuit	**a**
16	The K-map simplification for realisation of SR flip-flop from JK flip-flop is _____ a) J=1, K=0 b) J=R, K=S c) J=S, K=R d) J=0, K=1	**c**
17	Shift register is a___?	a

	a. Digital circuit b. Analog circuit c. Logic circuit d. Series circuit	
18	Which of the following is a disadvantage of shift registers? a. The memory size of a shift register is limited to the number of flip-flops used in the register b. The time required to access data from a shift register is more than that of a random access memory unit c. The reliability of the circuit decreases as its complexity increases d. None of above	a
19	Which of the following is a advantage of shift registers? a. The memory size of a shift register is limited to the number of flip-flops used in the register b. The time required to access data from a shift register is less than that of a random access memory unit c. The reliability of the circuit decreases as its complexity increases d. None of above	b
20	Which of the following statements are TRUE regarding shift registers? a. A shift register is a group of flip flops b. It is not used for data storage c. It is not used for the data movement d. Shift register includes set of latches	a

Set 9

Q.NO.		ANS
1	A half-adder does not have _____. A. carry in B. carry out C. two inputs D. all of the above	A
2	The output of an exclusive-NOR gate is 1. Which input combination is correct? A.A = 1, B = 0 B.A = 0, B = 1 C.A = 0, B = 0 D.none of the above	C
3	Before an SOP implementation, the expression $X = AB(\overline{C}D + EF)$ would require a total of how many gates? A. 1 B. 2 C. 4 D. 5	D
4	Assume you have A, B, C, and D available but not their complements. The minimum number of 2-input NAND gates required to implement the equation $X = A\overline{B} + B\overline{C}$ is _____. A. 3 B. 4	C

	C. 5 D. 6	
5	A gate can drive a number of load gate inputs up to its specified _____. A. supply voltage B. noise margin C. fan-in D. fan-out	D
6	The expression $A\overline{B} + \overline{A}B$ can be directly implemented using only _____. A. an XOR gate B. an XNOR gate C. an AOI circuit D. three 2-input NAND gates	A
7	The Boolean SOP expression obtained from the truth table below is _____.  A. $A\,B\,C + A\,B\,C$ B. $A\,\overline{B}\,C + A\,B\,\overline{C}$ C. $\overline{A}\,\overline{B}\,C + A\,B\,\overline{C}$ D. None of these	C
8		

Inputs			Output
A	B	C	X
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	0

9	For realisation of D flip-flop from SR flip-flop, the external input is given through _____ a) S b) R c) D d) Both S and R	**c**
10	How is JK flip-flop made to toggle a) J=0, K=0 b) J=1, K=0 c) J=0, K=1 d) J=1, K=1	**d**
11	Which of the following is correct for a gated D flip-flop? a) The output toggles if one of the inputs is held HIGH b) Only one of the inputs can be HIGH at a time c) The output complement follows the input when enabled d) Q output follows the input D when the enable is HIGH	**d**
12	What is the significance of the J and K terminals on the J-K flip-flop? a) There is no known significance in their designations b) The J represents jump, which is how the Q output reacts whenever the clock goes high c) The letters were chosen in honour of Jack Kilby, the inventory of the integrated circuit d) All of the other letters of the alphabet are already in use.	**c**
13	What is the meaning of D in D flip flop? a. Data b. Delay c. There is no specific meaning d. Both Data and Delay	**a**

14	Full form of T in T flip flop is a. Toggle b. Tolerate c. Trigger d. Both Toggle and Trigger	**a**
15	What is a trigger pulse? a. A pulse that starts a cycle of operation b. A pulse that reverses the cycle of operation c. A pulse that prevents a cycle of operation d. A pulse that enhances a cycle of operation	**a**
16	D flip flop can be made from a JK flip flop by making a. J=K' b. J=K=1 c. J=0, K=1 d. J=K	**a**
17	What is serial in parallel out (SIPO) shift register? a. Data is serial loaded into parallel output attached flip-flops b. Data is loaded into a single flip-flop and output appears parallel c. Data is loaded into serial output attached flip-flops and appear in serial order d. The data transmission can be done parallelly	b
18	Does a parallel-in serial-out (PISO) shift register configuration have the data input on lines D1 through D4 in parallel format, D1 being the ....bit? a. LSB b. MSB c. Data bit d. Binary digit	b

19	To write the data to the register, what must the Write/Shift control line be held? a. High b. Low c. Either d. Neither	b
20	In a Serial Input Serial Output, how is data is shifted? a. In SISO, a single bit is shifted at a time in either right or left direction under clock control b. In SISO, all bits are shifted at the same time in either right or left direction under clock control c. In SISO, the entire data is shifted at once in the same direction under clock control. d. None of the above	a